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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,152	02/06/2002	Sang-Eun Lee	8750-17	7500

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,152	LEE ET AL.	
	Examin r	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-20* is/are allowed.

6)☒ Claim(s) *1-10 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2-3 is objected to because of the following informalities: in line 2, the phrase "a first mark" should be changed to --the first mark-- to avoid a duplicant positive recitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamada et al (6559662).

Regarding claim 1; Yamada et al disclose [see Figs. 1-2] a method comprising: finding a location of a first defect (any x shown in Fig. 11) on a wafer (sample 14) using a semiconductor defect inspection instrument (electron beam exposing device 1); analyzing a composition of the first defect using the semiconductor defect inspection instrument (device 1 in combination with data processing device 4); and marking the location of the first defect (any x shown in Fig 11) on a wafer map (defective maps of Figs. 11-16) using a first mark (X in Fig. 12) to identify a type [large defect size see table 121 of Fig. 12] of the first defect [any x shown in Fig. 11].

Regarding claim 2, Yamada et al disclose [see Fig. 14] marking the location using the first mark (X) comprises using a first mark with a shape (shown as symbol A) that is dependent upon the type [size ranges of defect diameter see table 141 of Fig. 14] of the first defect.

Regarding claim 3, Yamada et al disclose [see Fig. 16] marking the location using the first mark (X) comprises using a first mark with a color (BROWN) that is dependent upon the type [size ranges of defect diameter see table 161 of Fig. 16 of the first defect.

Regarding claim 4, Yamada et al disclose [see Figs. 18-20] graphing a characteristic [hole diameter] of the first defect concurrently with marking the location on the wafer map [defective maps of Figs. 11-16].

Regarding claim 5, Yamada et al disclose [see Figs. 1-2] storing [via memory device 3] and analyzing [via data processing device 4] a characteristic [hole diameter] of the first defect (any x shown in Fig. 11) electronically using software [via control device 2].

Regarding claim 6, Yamada et al disclose [see Figs. 1-2] finding a location of a second defect (any x shown in Fig. 11) on the wafer (sample 14) using the semiconductor defect inspection instrument (electron beam exposing device 1); analyzing a composition of the second defect using the semiconductor defect inspection instrument (device 1 in combination with data processing device 4); and marking the location of the second defect (any x shown in Fig 11) on a wafer map (defective maps of Figs. 11-16) using a second mark (Y in Fig. 12) to identify a type [small defect size see table 121 of Fig. 12] of the second defect [any x shown in Fig. 11] using the first (X) and second (Y) marks to prepare a graph [see Figs. 18-20] to assist in statistically analyzing the first and second defects [any x shown in Fig. 11].

Regarding claim 7, Yamada et al disclose [see Figs. 7 and 11-16] a wafer defect map (DEFECTIVE MAP) comprising: a schematic representation [see Fig. 7] of a semiconductor wafer (sample 14) that includes demarcations (lines that form a square shape) corresponding to the location of chip boundaries; marking corresponding to a defect (any x in Fig. 11) on the semiconductor wafer (14), the marking identifying a type of the defect, a location of the marking (x) on the wafer map (10) corresponding to a location of the defect on the wafer (14).

Regarding claim 8, Yamada et al disclose [see Fig.16] the marking (x) configured to identify the type of the defect by using a color [example BROWN] that is associated with the type of the defect.

Regarding claim 9, Yamada et al disclose [see Fig.14] the marking (x) configured to identify the type of the defect by using a shape [example symbol A] that is associated with the type of the defect.

Regarding claim 10, Yamada et al discloses the location of the defect and the type of the defect (shown with x mark) is determined using a semiconductor defect inspection instrument (electron beam exposing device 1).

4. Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Simmons (6265232).

Regarding claim 21, Simmons disclose [see Figs. 1-2B] a method of statistically analyzing wafer defects (defect 14) on a semiconductor wafer (wafer 12) to improve yield, said method comprising: identifying a location and a type of the wafer defects (14) [represented in Fig. 1 as IDXXX also see step 20 in Fig. 2A]; determining a composition [yield loss] of the wafer defects (14), preparing a wafer defect map [see Fig. 1] to visually represent the location

and the type of the wafer defects (14), and preparing a bar graph [see Figs. 3-4] that represents a number of the wafer defects according to the type of the wafer defects (14).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Corley et al (5256578), La et al (5761064), Song (5838951), Miyazaki et al (6016562), Lovelace (6477685), and Nara et al (6567168) disclose a method and apparatus for marking a semiconductor wafer or device.

6. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

7. Claims 11-20 are allowed over the prior art.

8. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 11, in the examiner's opinion, it would not have been obvious to a person of ordinary skill in the art to determine a chemical composition of each of at least two defects on a semiconductor wafer of the prior art since the prior art only determine the size and location of any defects. Since claims 12-20 depend off of claim 11, they are also allowable.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (517) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
May 28, 2004